

Cache Allocation Technology (CAT)

A control system that supports Real-Time applications must ensure that the scheduling of control events happens in a deterministic manner.

Two key phenomena must be considered:

- Latency: The time between control events and their processing.
 It can be easily compensated and is comparable to a phase error.
- **Jitter:** The variability of latency over time. Due to its random nature, it cannot be compensated.

Sources of Jitter:

System Management Interrupt (SMI):

These are interrupts that execute BIOS code in System Management Mode (SMM) to perform tasks such as power management, USB legacy support, hardware monitoring, etc.

The handling of an SMI takes priority and effectively interrupts the execution of the operating system and all applications.

Shared Last Level Cache (LLC):

Modern processors share the last level of cache among various cores and the GPU.

Concurrent access to the last level of cache by all cores and the GPU can cause performance and determinism issues.

ASEM uses the Cache Allocation Technology (CAT) driver to optimize the use of the Last Level Cache (LLC).

CAT allows cores and the GPU to be exclusively assigned to specific portions of the cache. This eliminates interference with the cores used for Real-Time applications.

By using a Windows 10 64-bit kernel driver, ASEM has implemented the CAT Control Panel: an application that enables CAT programming tailored to customer needs.

The CAT Control Panel includes:

- A tab for each processor LLC group
- Two sliders for each core to adjust the assigned cache zones
- A graphical display that shows:
 - Shared cache zones (blue boxes)
 - Exclusive zones per core (green boxes)
- The amount of cache available per core
- The ability to import a CAT configuration from a .ccf file
- The ability to export a CAT configuration for use on another system



